Operation of the UniSLIC14™ and TCM38C17 Evaluation Module

Application Note | October 2001 | AN9931.1

Functional Description

This application note is intended to supplement Texas Instruments TCM38C17 EVM Users Guide. The Users guide describes three ways of evaluating the circuits operation:

- Using a TMS320C5402 DSK
- Using an analog signal generator and the TCM38C17 in digital loopback
- Using a Wandel and Golterman (W and G) PCM4

A good understanding of the material in the Users Guide is a prerequisite to this application note. For a detailed engineering analysis of the UniSLIC14 and TCM38C17 reference design, see application note AN9903.

This application note will evaluate the BASIC operation of the UniSLIC14 (Tests # 1- #7) and a system level evaluation (Tests # 8 and #9) using the PCM4. For discussion purposes, the TCM38C17 EVM board will be referred to as the Mother Board and the UniSLIC14 board will be referred to as the Daughter Board.

TCM38C17 Mother Board

The TCM38C17 Mother Board provides a way to evaluate the operation of Texas Instruments TCM38C17 Quad Combo and Intersil's UniSLIC14 family of SLICs. The following steps, repeated here from the Users Guide, will configure the mother board for testing Channel 0 with the PCM4:

- Connect TCM38C17, UniSLIC14 and PCM4 as shown in Figure 1.
- Configure the PCM4 general parameters per Table 1.
- Configure dipswitch SW7 as shown in Figure 2 for Channel 0 selected.
- Verify jumper JP1: Pin 2 shorted to Pin 3 (FPGA prom installed)
- Verify jumper JP2: open (CODEC output gain setting set by SLIC EVM)
- Verify jumper JP6: Open (external loopback not configured)
- Verify jumper JP7: Shorted (analog and digital grounds connected)
- Verify jumper JP8: Open (power supplied by external power supplies)
- Connect the external supplies to the Mother Board as shown in Table 2. Note: The Daughter Board gets its power from the Mother Board. If the design of the line card requires only one battery supply (-24V or -48V), then it is recommended that the -24V (V_{BL}) supply pin float.

Evaluation of channels 1-3 is accomplished by moving the daughter board to the desired channel and configuring SW7 to select that channel. SW7 selects the channel of the TCM38C17 that receives conversion data first. This will enable proper operation of the PCM4 once the transmit and receive channels are set to channel zero.

Daughter Board

The HC5514XEVAL3 evaluation board, due to the common pinout of the UniSLIC14 family, is capable of evaluating the performance of the following parts in the UniSLIC14 family (HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150).

The sample provided with this board (HC55142) will meet or exceed the electrical performance for all members of the family listed above. The board is configured to match a 600Ω line impedance, have a minimum loop current of 20mA, a maximum loop current of 30mA, onhook transmission of $0.775V_{RMS}$, offhook voice transmission of $3.2V_{PEAK}$, and a maximum loop resistance of 1777Ω.

For evaluation of the programmability of the HC5514 family, reference the data sheet for calculation of external components. An Excel spread sheet can be downloaded from the web for easy calculation of external components (www.intersil.com/telecom/unislic14.xls).

The daughter board is equipped with seven Single Pole Double Throw (SPDT) switches. Five of the logic control switches (C3, C2, C1, $\overline{SHD}$ and $\overline{GKD}/\overline{LVM}$) are center open toggle switches. If off-board mode control of the SLIC is desired, these switches can be set to center open position and driven by logic at the logic terminal port. The logic terminal port is located at the bottom right hand side of the daughter board, just above the VBL = VBL and POL/REV switches (reference Figure 4).

Features of the HC5514XEVAL3 Daughter Board

- Toggle Switch Programming for Logic States
- Monitoring of Switch Hook Detect ($\overline{SHD}$) and Ground Key / Line Voltage Measurement ($\overline{GKD}\_\overline{LVM}$) via On Board LEDs
- Selectable Power Sharing
- Single/Dual Battery Operation
- Logic Terminal Port for Easy Evaluation in Existing Systems
- Includes a Ring Relay for Evaluation of Ring Trip
- Selectable/Programmable Polarity Reversal Time
- Provisions for Line Voltage Measurement Test

Getting Started

Verify that the HC55142 is oriented in its socket correctly. Correct orientation is with pin 1 pointing towards the top of the board (64 pin connector (J4) to the right). (Reference the data sheet for device pinout.)

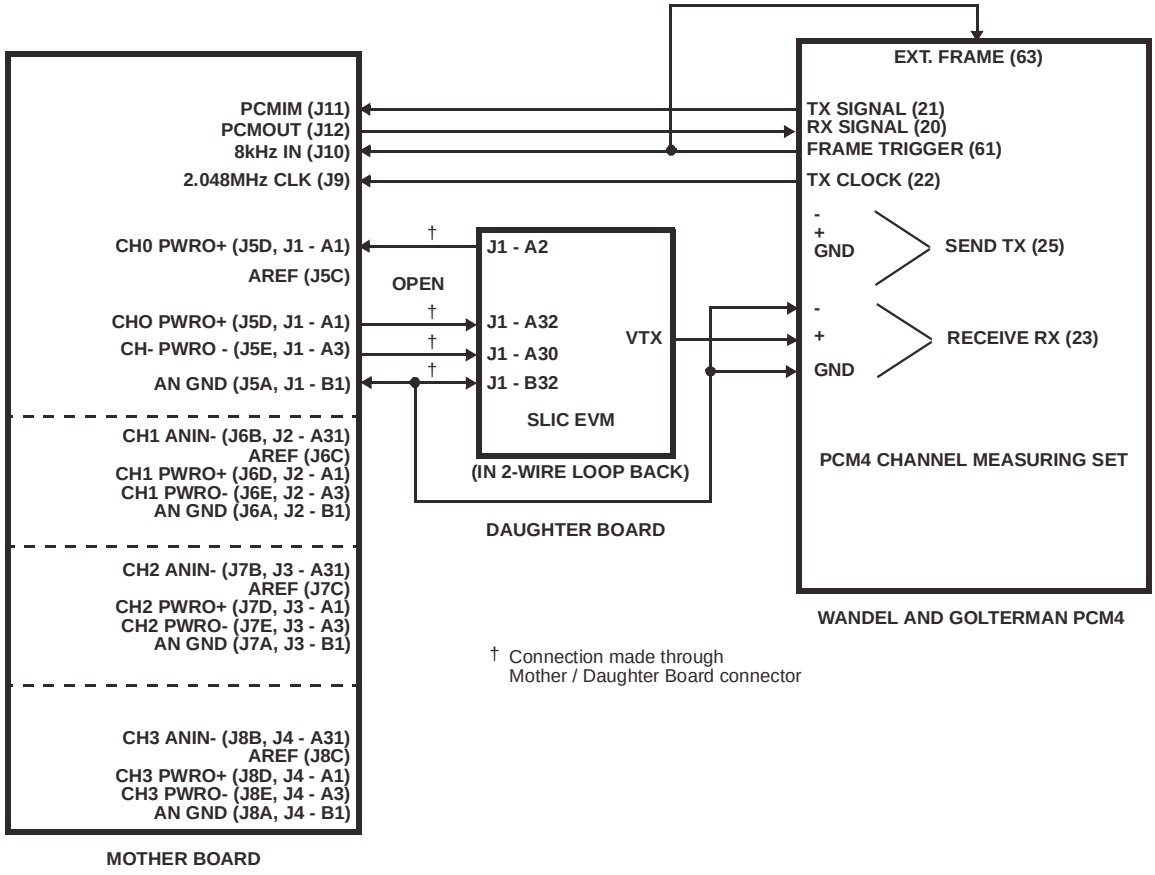

FIGURE 1. TCM38C17 CONNECTIONS TO PCM4 WITH UniSLIC14 EVM CONNECTED

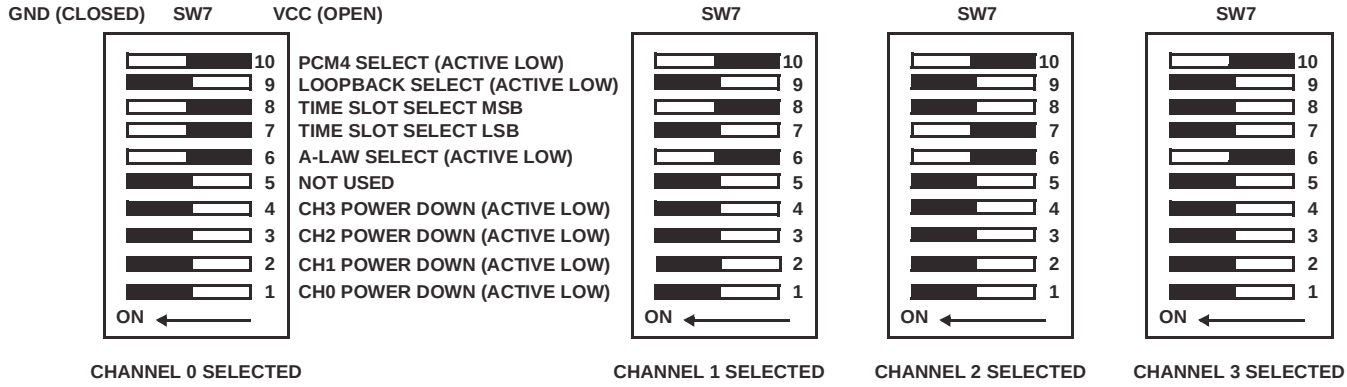

FIGURE 2. MOTHER BOARD SW7 DEFINITIONS AND CHANNEL SELECTION

TABLE 1. GENERAL PARAMETER SETTINGS IN THE PCM4

GENERAL PARAMETER	SETTING	ITEM NUMBER
(1) Digital Configuration		
General configuration	TX/RX 2M/2Mbits/s selected	11
Digital Loop (D - A)	2Mbits/s/all TS	21
(2) Frame Selection		
TX frame type	All 32 TS teleph	14
RX frame type	All 32 TS teleph	24
CRC-4 Multiframe	Off	31
(3) Digital TX Interface		
Line Code	75Ω unbalanced	13
Output Impedance	NRZ	22
Clock	Int. 2048 kHz	31
(4) Digital RX Interface		
Line Code	NRZ	13
Input Impedance	> 3kΩ	22
(5) Digital Words in TX Frame		
Frame Words	Reset to standard values	11
Send Signal	In select channels	21
(6) TX Error Insertion	Off	11
(7) PCM Coding		
TX Encoding Law	Must match switch S7-6 on TCM38C17 EVM. Default setting on EVM is A-law	11 to match EVM default
RX Encoding Law	Must match encoding law	21 to match EVM default
(8) Scanner Parameter		
VF-Input no.	1	11
VF-Output no.	1	21
(9) Special Parameter		
Level Display	dBm0	11
Two wire Term.	Infinite	13
Digital Channel no.	Time Slot	16

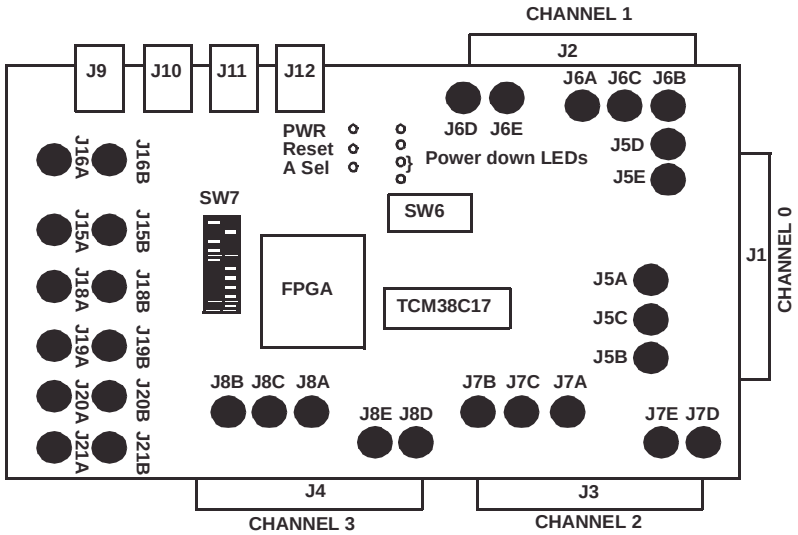

FIGURE 3. MOTHER BOARD LAYOUT

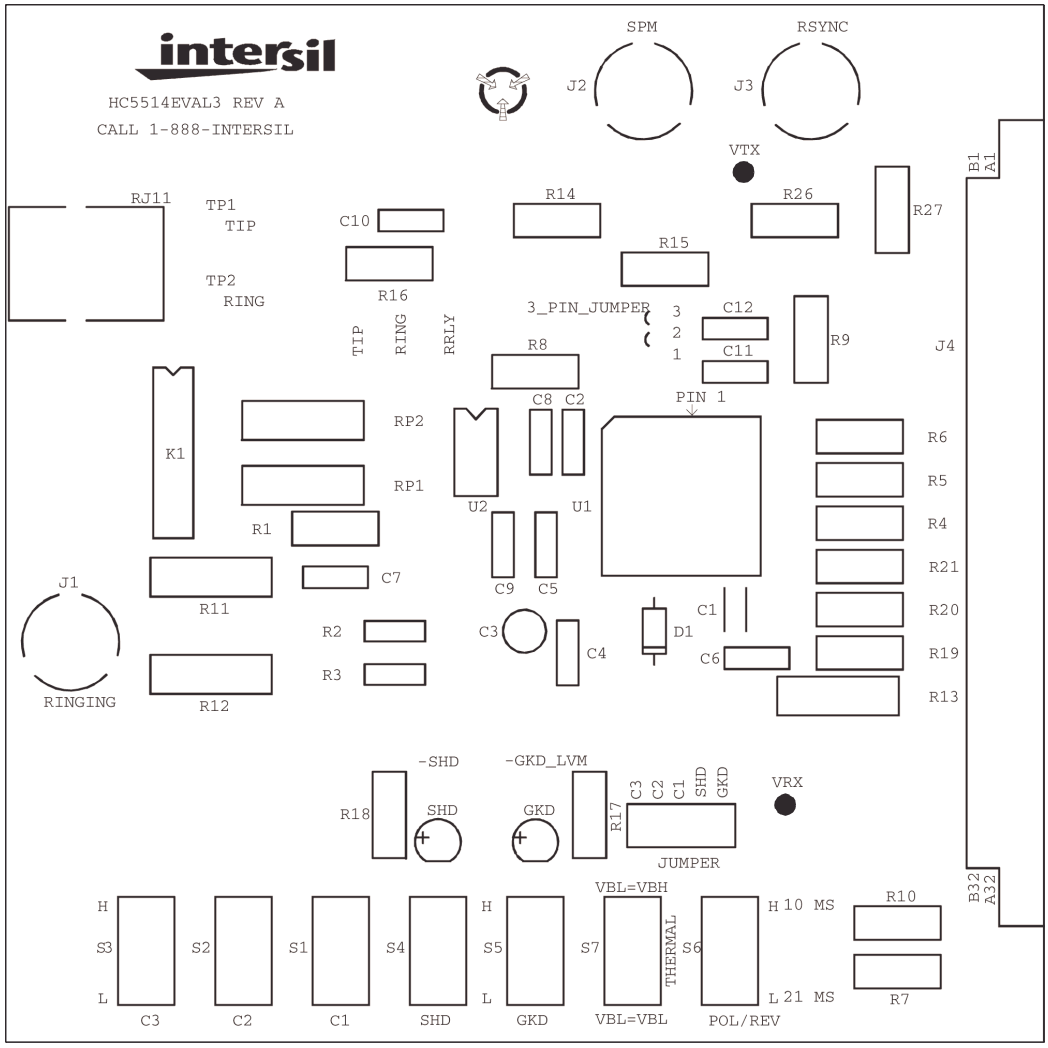

FIGURE 4. DAUGHTER BOARD LAYOUT

TABLE 2. POWER SUPPLY INTERFACE CONNECTIONS

POWER	CONNECTOR REFERENCE DESIGNATOR	REQUIRED BY
+5V Digital	J16A	TCM38C17 and Digital Circuits
Digital Ground	J16B	TCM38C17 and Digital Circuits
+5V Analog	J15A	TCM38C17 and SLICs
Analog Ground	J15B	TCM38C17 and SLICs
-24V	J18A	SLICs
-24V Ground	J18B	SLICs
-48V	J19A	SLICs
-48V Ground	J19B	SLICs

Operation and Performance of the Daughter Board

The operation and performance of the daughter board will be verified in two ways. The first will evaluate the operation of the daughter board itself, and the second will evaluate the operation of the daughter board and mother board in a system configuration.

The operation of the daughter board can be verified by performing the following tests:

1. Normal Loop Feed Verification
   Forward Active and Reverse Active States
2. Gain Verification
   4-Wire to 2-Wire and 2-Wire to 4-Wire
3. Polarity Reversal Time
4. Battery Selection/Power Sharing
5. Ring Trip Verification
6. Pulse Metering
7. Line Voltage Measurement Test

The evaluation of all 7 tests require the following equipment: a 600Ω (1 watt, 1%) load, a 1.5kΩ (2 watt, 1%) load, a 27.4kΩ (1/4 watt, 1%) RDC_RAC resistor, two sine wave generators, an AC/DC volt meter, three external supplies (V_{BH}, V_{BL}, V_{CC}), a dual channel storage oscilloscope, a telephone, BNC to banana adaptor, a battery backed AC source and a dynamic signal analyzer.

Test # 1 Normal Loop Feed Verification

This test verifies the correct tip and ring voltages in both onhook and offhook forward active and reverse active states. Loop current and ground key detect are also verified via the onboard $\overline{SHD}$ and $\overline{GKD}\_\overline{LVM}$ LEDs.

Discussion

The HC55142 is designed to have its most positive 2-wire terminal (tip in the forward active state and ring in the reverse active state) fixed at a set voltage. This set voltage depends upon the required overheads for the application. The most negative 2-wire terminals voltage is dependent upon the load across tip and ring and the programmable current limit.

The tip and ring voltages for various loop resistances are shown in Figure 5. The tip voltage remains relatively constant as the ring voltage moves to limit the loop current for short loops.

When power is applied to the SLIC, a loop current will flow from tip to ring through the 600Ω load. Loop current detection occurs when this loop current triggers an internal detector that pulls the output of $\overline{SHD}$ low, illuminating the LED through the +5V supply.

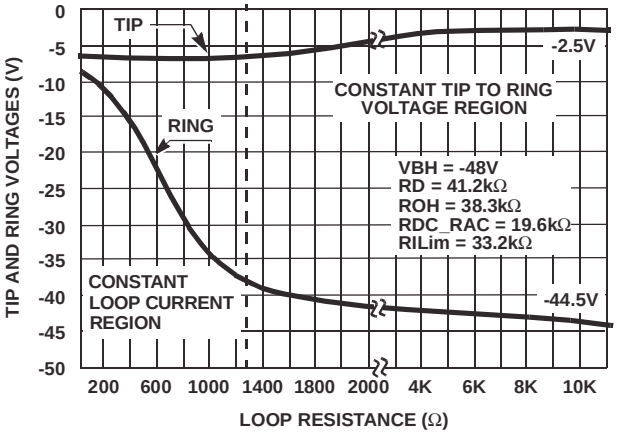

FIGURE 5. TIP AND RING VOLTAGES vs LOOP RESISTANCE

The Ground Key detector ($\overline{GKD}$) operation is verified by configuring the HC55142 in the tip open state and grounding the ring pin. Grounding the ring pin results in a current that triggers an internal detector that pulls the output of $\overline{GKD}\_\overline{LVM}$ low, illuminating the LED through the +5V supply.

Setup (Tip and Ring Voltages)

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LEDs illuminated).**
7. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
8. Configure SHD and GKD switches to be in the LED position (switch lever towards bottom of the board).
9. Using test ports TP1 (TIP) and TP2 (RING) located directly behind RJ11 jack, measure the tip and ring voltages with respect to ground and compare to those in Table 3 (onhook).
10. Terminate TP1 (TIP) and TP2 (RING) with a 600Ω load.
11. Measure tip and ring voltages with respect to ground and compare to those in Table 3 (offhook 600Ω).
12. Configure the SLIC to be in the Reverse Active State (C3 = 1, C2 = 1, C1 = 0).
13. Disconnect the 600Ω load from across TP1 and TP2.
14. Repeat steps 9 through 13.

TABLE 3. TIP AND RING VOLTAGES

LOGIC STATE	R_L (Ω)	TIP VOLTAGE REFERENCED TO GND	RING VOLTAGE REFERENCED TO GND
Forward Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	≅-2.5	≅-44.0
	Offhook 600Ω	≅-6.0	≅-24.0
Reverse Active V_{BH} = -48V V_{BL} = -24V V_{CC} = +5V	Onhook	≅-44.0	≅-2.5
	Offhook 600Ω	≅-24.0	≅-6.0

Verification of $\overline{SHD}$

1. With the SLIC in the forward active state, the $\overline{SHD}$ LED is on when tip and ring are terminated with 600Ω and off when tip and ring are an open circuit.

Verification of $\overline{GKD}$

1. Configure the SLIC to be in the Tip Open State (C3 = 1, C2 = 0, C1 = 0).
2. The $\overline{GKD}\_\overline{LVM}$ LED is on when ring is shorted to ground and off when ring is an open circuit. Notice that the $\overline{SHD}$ LED will also be on.

Test # 2 Gain Verification

This test will verify the SLIC is operating properly and that the 4-wire to 2-wire gain (Equation 1) is -1.0 (0.0dB). +PWRO = V_{RX}

$$A_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_{TR}} = -2\frac{Z_L}{Z_L + \left(\frac{Z_T}{200} + 2R_P\right)} \quad \text{(EQ. 1)}$$

The programmable 2-wire to 4-wire transmission gain (Equation 2) will also be verified by measuring the SLIC's 4-wire to 4-wire gain with the PTG pin floating ($A_{2\text{-}4}$ is 0.9 (0.91dB) and grounded ($A_{2\text{-}4}$ is 0.56 (-5.0dB).)

$$A_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_{TR} - 2R_P}{Z_{TR}} \quad \text{(EQ. 2)}$$

Discussion

When tip and ring are terminated with 600Ω load, the SLIC will exhibit unity gain from the 4-wire VRX input pin to across the 2-wire tip and ring pins (V_{TR}). When an open circuit exists, a mismatch occurs and the tip to ring voltage doubles.

An easy way to measure the 2-wire to 4-wire transmit gain, without a floating signal generator on the 2-wire side, is to use the signal from the PCM4 through the mother board and measure the 4-wire to 4-wire gain. Given that the 4-wire to 2-wire gain is approximately one, it follows that the 2-wire to 4-wire transmission gain is also approximately equal to the 4-wire to 4-wire gain. The dB 4-wire to 4-wire gain is calculated in Equation 3.

$$dB_{4W-4W} = 20\log\frac{V_{TX}}{V_{RX}} \quad \text{(EQ. 3)}$$

Setup (4-Wire to 2-Wire Gain)

If previous test was Test #1, skip to step 7.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LEDs will turn off.
8. Configure the PCM4 for the MODE A11 test. Set the level to 0dBm0. Set PCM4 to D-A. Set the frequency to 1004Hz. This will provide a 1kHz 1V_{RMS} signal at the VRX input to the SLIC.
9. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
10. Using test ports TP1 (TIP) and TP2 (RING) located directly behind RJ11 jack, terminate tip and ring with a 600Ω load.
11. Connect an AC voltmeter across tip and ring.

Verification

1. Tip to ring AC voltage of 1V_{RMS} when terminated with a 600Ω load. The dB ($A_{4\text{-}2}$) gain is approximately 0dB.
2. Tip to ring AC voltage of 2V_{RMS} when not terminated. The dB ($A_{4\text{-}2}$) gain is approximately 6dB.
3. Configure the SLIC to be in the Reverse Active state (C3 = 1, C2 = 1, C1 = 0) and repeat above test.

Setup (2-Wire to 4-Wire Gain)

If previous test was test #2a, skip to step 9.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board. Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LEDs will turn off.
8. Configure the PCM4 for the MODE A11 test. Set the level to 0dBm0. Set PCM4 to D-A. Set the frequency to 1004Hz. This will provide a 1kHz 1V_{RMS} signal at the VRX input to the SLIC.
9. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
10. Using test ports TP1 (TIP) and TP2 (RING) located directly behind RJ11 jack, terminate tip and ring with a 600Ω load.
11. Verify that pin 2 of the 3_PIN_JUMPER (located towards the middle of board near the upper left hand corner of the SLIC) is floating (Figure 4). This condition floats the PTG pin. Reference section titled "Layout Considerations" for more information about the PTG pin.
12. Connect an AC voltmeter, referenced to ground, to the VTX output (test point located near top right hand side of board Figure 4).

Verification

1. VTX voltage of 1.1V_{RMS} when pin 2 of the PTG jumper is floating. The dB ($A_{2\text{-}4}$) gain is approximately 0.9dB.
2. VTX voltage of 0.55V_{RMS} when pin 2 of the PTG jumper is shorted to pin 1, via the supplied jumper. This condition grounds the PTG pin. The dB ($A_{2\text{-}4}$) gain is approximately -5.0dB.
3. Configure the SLIC to be in the Reverse Active state (C3 = 1, C2 = 1, C1 = 0) and repeat above test.

Test # 3 Polarity Reversal Time

This test will illustrate the operation and programming of the polarity reversal feature.

Discussion

The HC55142 has a programmable polarity reversal time. The evaluation board is equipped with a toggle switch for evaluation of a 10µs and 20µs reversal times. Equation 4 gives the formula for programming a desired reversal time.

$$RSYNC\text{–}REV = (3.47k\Omega)(ReversalTime(ms)) \quad \text{(EQ. 4)}$$

$$34.7k\Omega < RSYNC\text{–}REV > 73.2k\Omega$$

C4 and R7/R10 set the timing for the polarity reversal time. It is recommended that programming of the reversal time be accomplished by changing the value of R7/R10 (see Figure 9).

Setup

If previous test was either test #1 or #2, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. Turn off power to the system to reset the mother board so all channels are in power-down state after power is applied.
7. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LEDs illuminated).**
8. Configure the SLIC to be in the Forward Active State (C3 = 0, C2 = 1, C1 = 0).
9. Verify that the POL/REV pin S6 (lower right hand side of the board) is in either the 10ms or 20ms position.
10. Using test ports TP1 (TIP) and TP2 (RING) located directly behind RJ11 jack, terminate tip and ring with a 600Ω load.
11. Select either 10µs or 20µs polarity reversal time via the POL / REV switch at the bottom right hand side of the board.
12. Monitor the tip and ring voltage levels with a dual channel storage scope. Toggle the SLIC between the Forward Active state and the Reverse Active states to trigger the scope.
13. Measure the time of reversal. Compare results to that listed in Table 4.
14. Switch the POL / REV (S6) switch to the other reversal time and compare results to that listed in Table 4.

TABLE 4. POLARITY REVERSAL TIME

POLARITY REVERSAL SWITCH SETTING	FORWARD ACTIVE TO REVERSE	REVERSE ACTIVE TO FORWARD
10µs	≈10µs	≈10µs
20µs	≈20µs	≈20µs

Test # 4 Battery Selection/Power Sharing

Discussion (Battery Selection)

The following is a theoretical discussion that will illustrate the automatic switching of the supplies. Figure 6 was generated by monitoring the V_{BH} and V_{BL} supply currents for various tip and ring loads.

Battery selection is a technique, for a two battery supply system, where the SLIC automatically diverts the loop current to the most appropriate supply for a given loop length. This results in significant power savings and lowers the total power consumption on short loops. This technique is particularly useful if most of the lines are short, and the on hook condition requires a -48V battery. In Figure 6, it can be seen that for long loops the majority of the current comes for the high battery supply (V_{BH}) and for short loops from the low battery supply (V_{BL}).

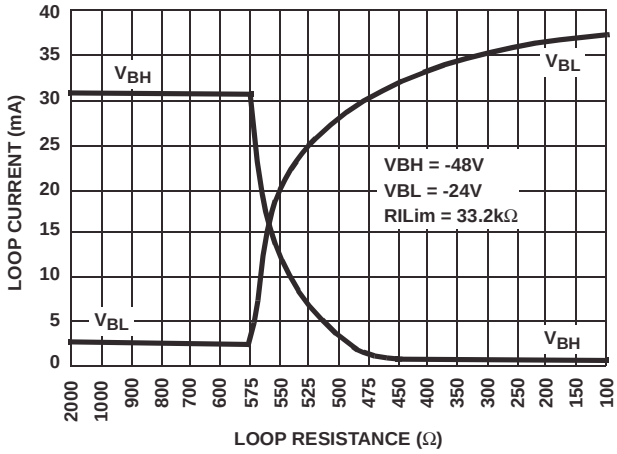

FIGURE 6. BATTERY SELECTION (DUAL SUPPLY SYSTEMS)

Verification

1. Notice for the onhook condition (extremely long line) that all the current is provided by V_{BH}. This feature enables onhook transmission on the longest loop for a given battery voltage.
2. Notice for a 600Ω load, the current is shared by both V_{BH} and V_{BL}. If tip and ring are shorted, then most of the loop current will come from V_{BL}.
3. Notice the same is true for the reverse active state.

Discussion (Power Sharing)

Power sharing is a method of redistributing the power away from the SLIC in short loop applications. The total system power is the same, but the die temperature of the SLIC is much lower. Power sharing becomes important if the application has a single battery supply (-48V on hook requirements for faxes and modems) and the possibility of high loop currents (reference Figure 6). This technique would prevent the SLIC from getting too hot and thermally shutting down on short loops.

The power dissipation in the SLIC is the sum of the smaller quiescent supply power and the much larger power that results from the loop current. The power that results from the loop current is the loop current times the voltage across the SLIC. The power sharing resistor (R_{PS}) reduces the voltage across the SLIC, and thereby the on-chip power dissipation. The voltage across the SLIC is reduced by the voltage drop across R_{PS}. This occurs because R_{PS} is in series with the loop current and the negative supply.

A mathematical verification follows:

Given: $V_{BH} = V_{BL}$ = -48V, Loop current = 30mA, R_L (load across tip and ring) = 600Ω, Quiescent battery power = (48V) (0.8mA) = 38.4mW, Quiescent VCC power = (5V) (2.7mA) = 13.5mW, Power sharing resistor = 600Ω.

1. Without power sharing, the on-chip power dissipation would be 952mW (Equation 5).
2. With power sharing, the on-chip power dissipation is 412mW (Equation 6). A power redistribution of 540mW.

On-chip power dissipation without power sharing resistor.

$$P_D = (V_{BH})(30mA) + 38.4mW + 13.5mW - (RL)(30mA)^2$$

$$P_D = 952mW \quad \text{(EQ. 5)}$$

On-chip power dissipation with 600Ω power sharing resistor.

$$P_D = (V_{BH})(30mA) + 38.4mW + 13.5mW - (R_L)(30mA)^2 - (R_{PS})(30mA)^2$$

$$P_D = 412mW \quad \text{(EQ. 6)}$$

The design trade-off in using the power sharing resistor is loop length verses on-chip power dissipation.

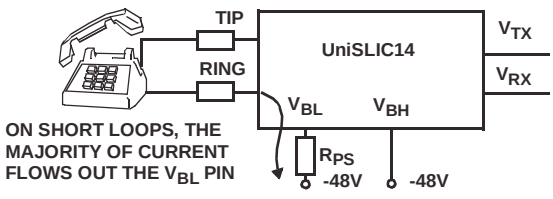

FIGURE 7. POWER SHARING (SINGLE SUPPLY SYSTEMS)

Test # 5 Ring Trip Verification

This test will verify the ringing function of the HC5514X. A telephone, a battery referenced AC signal source, and a BNC to banana adaptor are the only additional hardware required to complete the test.

Discussion

The 600Ω termination is not necessary for this test since the phone provides this nominal impedance when offhook. If the RSYNC_REV pin is grounded, the ring relay driver pin (RRLY) pin goes low after the SLIC is placed in the ringing state. This will energize the ring relay. The ring relay disconnects tip and ring from the phone and connects the path for the ringing signal. The D_T and D_R comparator inputs will sense the flow of DC loop current, enabling the ring trip comparator to sense when the phone is either onhook or offhook. When an offhook condition is detected, the HC55142 will automatically disconnect the ringing signal to the phone at zero current crossing. This reduces impulse noise to the system.

Setup

If previous test was either test #1 or #3, skip to step 8.
If previous test was test #2, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. Turn off power to the system to reset the mother board so all channels are in power-down state after power is applied.
7. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LEDs illuminated).**
8. Configure the SLIC to be in the Ringing State (C3 = 0, C2 = 0, C1 = 1).
9. Configure S4 and S5 to be in the LED position (switch lever towards bottom of board). Reference Figure 4.
10. Connect the telephone across tip and ring via the RJ11 jack on the daughter board.
11. Connect battery backed AC (20Hz, 90V_{RMS} +V_{BH}) source to “RINGING” located below the RJ11 jack.

Verification

1. Phone starts ringing when power is applied to the test setup; if not, toggle C1.
2. While ringing and Onhook, $\overline{SHD}$ LED is not illuminated.

3. While ringing, going offhook will illuminate the $\overline{SHD}$ LED. When an offhook condition is detected, the HC55142 will automatically disable the RRLY pin (pin goes high) at zero current crossing. This will disable the ring relay and reconnect the tip and ring lines to the phone.
4. When the phone is returned to the Onhook condition, SHD light will remain on until the logic state of the SLIC is changed. This precludes any false on hook detection during the transition between off hook (during ringing) and the off hook active state.

Test # 6 Pulse Metering

This test will verify that an offhook $3.1V_{PEAK}$ pulse metering signal and a $1.1V_{PEAK}$ voice signal can be transmitted simultaneously across a complex loop resistance, on tip and ring, with less than 1% Total Harmonic Distortion. The complex loop impedance is equal to 200Ω at the pulse metering frequency of 16kHz, and consist of a series 200Ω resistor and a parallel combination of an 820Ω resistor and a 0.1µF capacitor. Programming of the offhook overhead voltage required for simultaneously operation of both signals is achieved by changing the value of RDC_RAC to 27.4kΩ.

A 27.4kΩ RDC_RAC resistor, two signal generators, the complex load listed above and a dynamic signal analyzer are required to complete this test.

Setup

If previous test was either test #1, #3 or #5, skip to step 8.
If previous test was test #2, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. Turn off power to the system to reset the mother board so all channels are in power-down state after power is applied.
7. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LEDs illuminated).**
8. Configure the SLIC to be in the Forward Active state (C3 = 0, C2 = 1, C1 = 0).
9. Change R1 resistor RDC_RAC to 27.4kΩ.
10. Verify that pin 2 of the 3_PIN_JUMPER (located towards the middle of board near the upper left hand corner of the SLIC) is shorted to pin 1 (Figure 4). This condition grounds the PTG pin. Reference section titled “Layout Considerations” for more information about the PTG pin.
11. Connect a series 200Ω resistor and a parallel combination of an 820Ω resistor and a 0.1µF capacitor across tip and ring terminals.
12. Put a $0.777V_{RMS}$ ($1.1V_{PEAK}$) 1kHz signal into the VRX input (lower right hand corner of daughter board, Figure 4).
13. Put a $0.55V_{RMS}$ 16kHz signal into the SPM input (located at top of daughter board). $0.55V_{RMS}$ is equivalent to $3.1V_{PEAK}$ across tip and ring due to gain of 4 from the SPM pin to tip and ring.
14. Measure the THD across the complex test load.

Verification

1. The THD of the 1kHz signal is less than 1%.

Test # 7 Line Voltage Measurement

Discussion

A few of the SLICs in the UniSLIC14 family feature Line Voltage Measurement (LVM) capability. This feature provides a pulse on the $\overline{GKD}\_\overline{LVM}$ output pin that is proportional to the loop voltage. Knowing the loop voltage and thus the loop length, other basic cable characteristics such as attenuation and capacitance can be inferred. Decisions can be made about gain switching in the CODEC to overcome line losses and verification of the 2-wire circuit integrity.

The LVM function can only be activated in the off hook condition in either the forward or reverse operating states. The LVM uses the ring signal supplied to the SLIC as a time base generator. The loop resistance is determined by monitoring the pulse width of the output signal on the $\overline{GKD}\_\overline{LVM}$ pin. The output signal on the $\overline{GKD}\_\overline{LVM}$ pin is a square wave for which the average duration of the low state is proportional to the average voltage between the tip and ring terminals. The loop resistance is determined by the tip to ring voltage and the constant loop current. Reference Figure 8.

Although the logic state changes to the Test Active State when performing this test, the SLIC is still powered up in the active state (forward or reverse) and the subscriber is unaware the measurement is being taken.

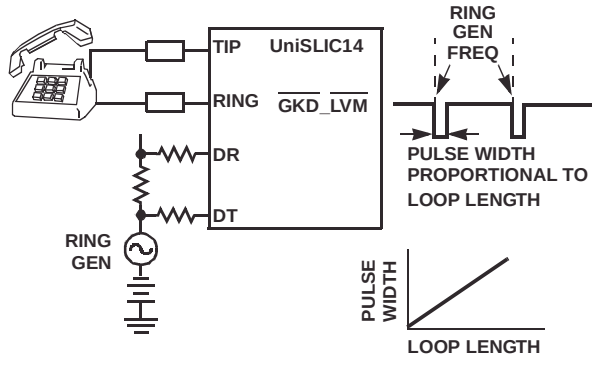

FIGURE 8. OPERATION OF THE LINE VOLTAGE MEASUREMENT CIRCUIT

Setup

If previous test was either test #1, #3, #5 or #6 skip to step 8.
If previous test was test #2, skip to step 6.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V).
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. Turn off power to the system to reset the mother board so all channels are in power-down state after power is applied.
7. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3). **This test will be preformed with all channel from the mother board in the power down condition (all LEDs illuminated).**
8. Using test ports TP1 (TIP) and TP2 (RING) located directly behind RJ11 jack, terminate tip and ring with a 600Ω load.
9. Configure the SLIC to be in the Test Active State (C3 = 0, C2 = 1, C1 = 1).
10. Connect battery backed AC (20Hz, 90V_{RMS} +V_{BH}) source to RING GEN INPUT located just below the tip and ring terminals on the board.
11. Verify that pin 2 of the 3_PIN_JUMPER (located towards the middle of board near the upper left hand corner of the SLIC) is floating (Figure 4). This condition floats the PTG pin. Reference section titled “Layout Considerations” for more information about the PTG pin.
12. Monitor the output signal on the $\overline{GKD}\_\overline{LVM}$ pin with a scope.

Verification

1. The output signal on the test port $\overline{GKD}\_\overline{LVM}$ pin (located just above the GKD LED) is a square wave for which the average duration of the low state is proportional to the average voltage between the tip and ring terminals.
2. Change the load to 1.5kΩ load and notice the change in the pulse width of the $\overline{GKD}\_\overline{LVM}$ pulse.
3. Notice the same is true for the Test Reversal Active State (C3 = 1, C2 = 1, C1 = 1).

Test # 8 Variable Gain / Frequency

This test will configure the HC55142 in the loopback mode and evaluate the TCM38C17 and the UniSLIC14’s AC performance across frequency.

Discussion

Most of the SLICs in the UniSLIC14 family feature 2-Wire loopback testing. This loopback function is only activated when the subscriber is **on hook** and the logic command to the SLIC is in the Test Active State. (Note: if the subscriber is **off hook** and in the Test Active State, the function performed is the Line Voltage Measurement.)

During the 2-wire loopback test, a 2kΩ internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{SHD}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested. Together with the 4-wire loopback test in the Open Circuit logic state, this 2-wire loopback test allows the complete network (including SLIC) to be tested up to the subscriber loop.

Setup

If previous test was test #2, skip to step 8.
If previous test was either test #1, #3, #5, #6 or #7, skip to step 7.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LEDs will turn off.
8. Configure the SLIC to be in the Loopback State (C3 = 0, C2 = 1, C1 = 1).
9. Configure the PCM4 for the MODE A 33 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test part.

Verification

Compare results to the Figure 9.

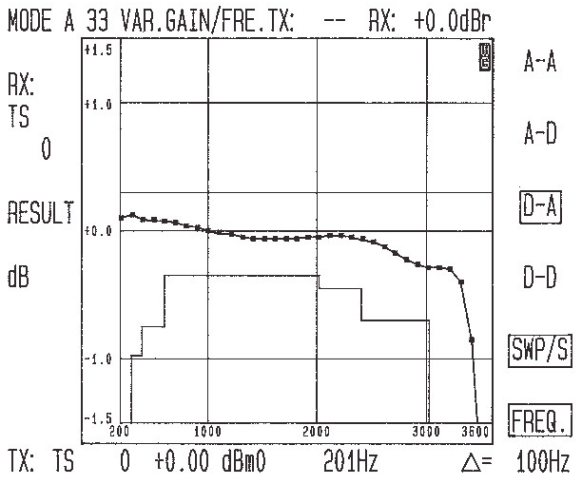

FIGURE 9. VARIABLE GAIN vs FREQUENCY

Test # 9 Total Distortion

This test will configure the HC55142 in the loopback mode and evaluate the TCM38C17 and the UniSLIC14's Total Distortion.

Discussion

Most of the SLICs in the UniSLIC14 family feature 2-Wire loopback testing. This loopback function is only activated when the subscriber is **on hook** and the logic command to the SLIC is in the Test Active State. (Note: if the subscriber is **off hook** and in the Test Active State, the function performed is the Line Voltage Measurement.)

During the 2-wire loopback test, a 2kΩ internal resistor is switched across the tip and ring terminals of the SLIC. This allows the $\overline{SHD}$ function and the 4-wire to 4-wire AC transmission, right up to the subscriber loop, to be tested. Together with the 4-wire loopback test in the Open Circuit logic state, this 2-wire loopback test allows the complete network to be tested up to the subscriber loop.

Setup

If previous test was either test #2 or #8, skip to step 8.
If previous test was either test #1, #3, #5, #6 or #7, skip to step 7. If previous test was test #8, skip to step 9.

1. Configure mother board for testing channel 0 with the PCM4. Reference Figure 2.
2. Connect daughter board to port J1 of mother board Reference Figure 3.
3. Apply power to the system (apply 5V then -24V and -48V) and turn on the PCM4.
4. Verify supply voltages V_{BH} (J19A) = -48V, V_{BL} (J18A) = -24V and V_{CC} (J15A, J16A) = +5V.
5. Set S7 in the VBL = VBL position (switch lever towards bottom of board). Reference Figure 4.
6. All of the channel power-down LEDs will be illuminated along with the PWR LED and the A SEL LED (Figure 3).
7. Press the TCM38C17 reset switch (SW6). The channel power-down LEDs will turn off.
8. Configure the SLIC to be in the Loopback State (C3 = 0, C2 = 1, C1 = 1).
9. Configure the PCM4 for the MODE A 51 test. Set PCM4 to D-A, SWP/S (single sweep). Press start to test part.

Verification

Compare results to that shown in Figure 10.

Layout Considerations

Systems with Dual Supplies (V_{BH} and V_{BL})

If the V_{BL} supply is ***not*** derived from the V_{BH} supply, it is recommended that an additional diode be placed in series with the V_{BH} supply. The orientation of this diode is anode on pin 8 of the device and cathode to the external supply. This external diode will inhibit large currents and potential damage to the SLIC, in the event the V_{BH} supply is shorted to GND. If V_{BL} is derived from V_{BH} then this diode is not required.

Floating the PTG Pin

The PTG pin is a high impedance pin (500kΩ) that is used to program the 2-wire to 4-wire gain to either 0dB or -6dB.

If 0dB is required, it is necessary to float the PTG pin. The PC board interconnect should be as short as possible to minimize stray capacitance on this pin. Stray capacitance on this pin forms a low pass filter and will cause the 2-wire to 4-wire gain to roll off at the higher frequencies.

If a 2-wire to 4-wire gain of -6dB is required, the PTG pin should be grounded as close to the device as possible.

SPM Pin

For optimum performance, the PC board interconnect to the SPM pin should be as short as possible. If pulses metering is not being used, then this pin should be grounded as close to the device pin as possible.

RLIM Pin

The current limiting resistor R_{LIM} needs to be as close to the RLIM pin as possible.

Layout of the 2-Wire Impedance Matching Resistor Z_T

Proper connection to the Z_T pin is to have the external Z_T network as close to the device pin as possible.

The Z_T pin is a high impedance pin that is used to set the proper feedback for matching the impedance of the 2-wire side. This will eliminate circuit board capacitance on this pin to maintain the 2-wire return loss across frequency.

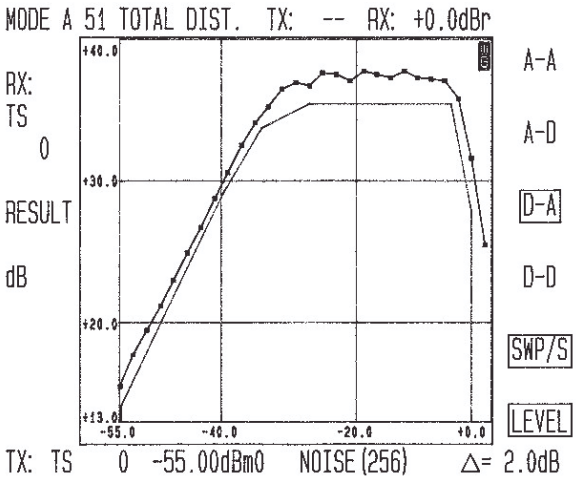

FIGURE 10. TOTAL DISTORTION

Demo Board Schematic

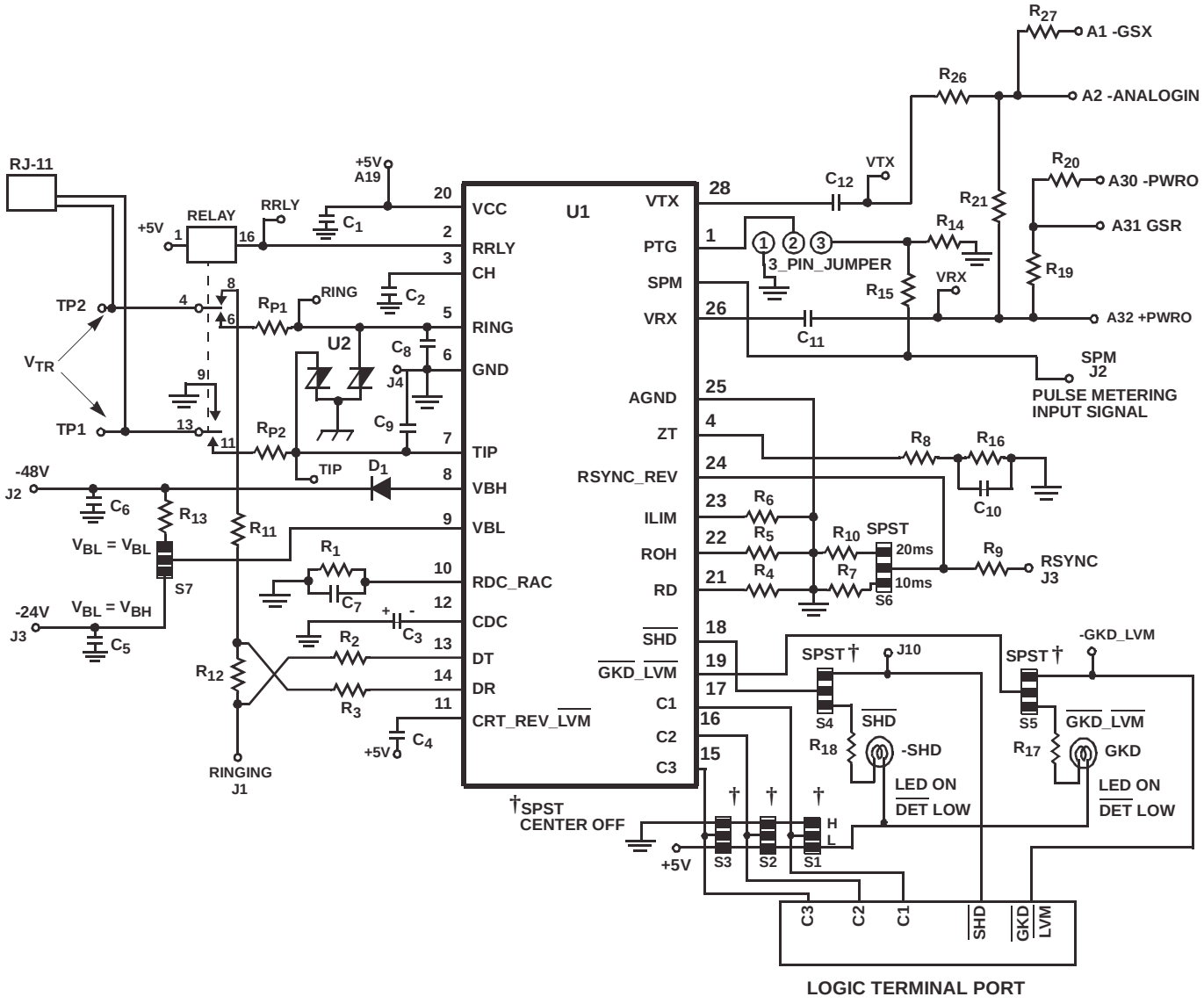

FIGURE 11. UniSLIC14 DEMO DAUGHTER BOARD SCHEMATIC

TABLE 5. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1082F3	N/A	N/A
RP1, RP2 (Line Feed Resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RAC) R = 50*RFEED, RFEED = 381Ω	21.0kΩ	1%	1/16W
R2, R3 (Input Current Limiting Resistors for DT and DR)	2MΩ	1%	1/16W
R4 (RD Resistor) R = 500/I_{SH}, I_{SH} = 9.78mA	41.2kΩ	1%	1/16W
R5 (ROH Resistor) R = 500/Iloop(Min)-I_{SH}- (Iloop(Min) = 20mA, I_{SH}- 6.54mA)	38.3kΩ	1%	1/16W
R6 (R_{ILIM} Resistor) R = 1000/ILIM (ILIM = 30mA)	33.2kΩ	1%	1/16W
R7 (RSYNC_REV Resistors) R = 3.47k/µs (10µs)	34.8kΩ	1%	1/16W

TABLE 5. BASIC APPLICATION CIRCUIT COMPONENT LIST (Continued)

COMPONENT	VALUE	TOLERANCE	RATING
R8 (RZT, 2-Wire Impedance Matching Resistor) R = 200(ZO-2RF) Z0 = 600Ω, RF = 30Ω	107Ω	1%	1/4W
R9 (Current Limit Resistor for Ring Sync Pulse)	49.9kΩ	1%	1/16W
R10 (RSYNC_REV Resistor) R = 3.47k/µs (21µs)	69.8kΩ	1%	1/16W
R11 (Series Resistor to Simulate Loop Length During Ringing)	600Ω	1%	2W
R12 (Sense Resistor for DC Current During Ringing)	400Ω	1%	2W
R13 (R_{PS}, Power Sharing Resistor)	Open	-	-
R14, R15 (Pulse Metering Transhybrid Resistors)	10kΩ	1%	1/16W
R16, C10 (For Matching a Complex 2-Wire Impedance)	R = 0Ω C10 = Open	-	-
R17, R18 (Current Limiting Resistors for LEDs)	1kΩ	5%	1/4W
R19 (Receive Gain of TCM38C17 Programming Resistor) G=1	Open	1%	1/4W
R20 (Receive Gain of TCM38C17 Programming Resistor) G=1	0Ω	1%	1/4W
R21 (Voice Path Transhybrid Resistor)	48.7kΩ	1%	1/4W
R26 (Voice Path Transhybrid Resistor)	53.6kΩ	1%	1/4W
R27 (Voice Path Transhybrid Resistor)	60.4kΩ	1%	1/4W
C1, C5	0.1µF	20%	50V
C2	0.1µF	20%	10V
C3	4.7µF	10%	50V or (V_{BH}/2)
C4, C7, C11, C12	0.47µF	20%	10V
C6	0.1µF	20%	100V
C8, C9	2200pF	20%	100V
$\overline{SHD}$ and $\overline{GKD}$_$\overline{LVM}$ LEDs	Red	-	-
D1, Recommended if the V_{BL} supply is not derived from the V_{BH} supply.	1N4004	-	-

Design Parameters: Switch Hook Threshold = 12mA, Loop Current Limit = 30mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

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